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REDUCED THICKNESS VARIATION IN A MATERIAL LAYER DEPOSITED IN NARROW AND WIDE INTEGRATED CIRCUIT TRENCHES

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BACKGROUND

1. Field of invention

Depositing material in trenches formed in integrated circuit substrates, and in particular reducing the thickness variations of a silicon dioxide layer deposited in narrow and wide substrate trenches using a high density plasma chemical vapor deposition process.

2. Related art

In a typical integrated circuit, electrically active areas are formed in a semiconductor substrate. The active areas are separated by electrical insulation regions. One method of forming such insulation regions is shallow trench isolation (STI).

In a typical STI process, a silicon nitride layer is deposited over a monocrystalline silicon substrate. One or more other layers (e.g., polycrystalline silicon) may exist between the silicon nitride and the substrate. The silicon nitride layer is patterned to cover the active areas, but not the areas in which the insulation regions are to be formed. Trenches are etched in the substrate (and in overlying layers, if any) at insulation region locations. Then, an insulating layer of silicon dioxide (SiO_2) is deposited. The silicon dioxide covers the silicon nitride and fills the trenches. Next, chemical-mechanical polishing (CMP) is used to remove the deposited silicon dioxide overlying the silicon

nitride. The CMP stops at the silicon nitride, and the trenches remain filled with silicon dioxide. Finally, an etch (e.g., wet anisotropic etch using hydrofluoric acid) is performed.

A High Density Plasma Chemical Vapor Deposition (HDP-CVD) process is used to deposit the SiO_2 in the trenches. The HDP-CVD process differs from Plasma Enhanced Chemical Vapor Deposition (PECVD) and low pressure Chemical Vapor Deposition (CVD). In HDP-CVD, the ion flux to the substrate surface on which material is deposited is larger than the net deposition flux to the surface. As a result, the deposited SiO_2 film is more dense and has less hydrogen incorporation as compared to an SiO_2 film deposited using PECVD. In addition, the HDP-CVD ion flux assists sputtering and oxide etch at the upper trench corners. A low pressure Chemical Vapor Deposition (CVD) process must be done in a furnace at high temperatures (typically above 700 °C) to thermally deposit SiO_2 on the substrate. In contrast, HDP-CVD requires plasma to break down the gas species so that their components will form SiO_2 on the substrate surface.

Isolation trenches may be characterized by an aspect ratio, which is the ratio of trench depth to trench width (depth divided by width). HDP-CVD is used for sub-micron ultra large scale integration (ULSI) technologies due to its high aspect ratio (more than 4:1) trench fill capability as compared with, for example, a low pressure CVD process.

A SPEED model tool, manufactured by NOVELLUS, Inc. of San Jose, California, can be used to deposit silicon dioxide in an HDP-CVD STI process. The substrate on which the silicon dioxide is to be deposited is placed in the tool's reaction chamber. A mixture of silane (SiH_4), oxygen (O_2), and inert (e.g., argon (Ar) or helium (He)) gasses is

introduced into the reaction chamber. The silane and oxygen react to form silicon dioxide and hydrogen.

When a plasma (glow discharge) is formed in the reaction chamber, the HDP-CVD process deposits material. In many instances the HDP-CVD process also sputter etches at least a part of the deposited material. A low frequency (e.g., 400 kiloHertz (kHz)) radio frequency (RF) signal is established between an electrode and the substrate and creates the plasma ions. In addition, a high frequency (HF)(e.g., 13.56 MegaHertz (MHz)) bias signal is established between the electrode and the substrate. The HF bias signal attracts positive ions (e.g., He^+ ions) used to resputter oxide deposited at the top corners (cusps) of the trenches, and the resputtered oxide helps to fill the trench. The ion current results in a DC potential between the electrode (anode) and the substrate (cathode).

For trenches of equal depth, a wide trench's volume to be filled with oxide is larger than a narrow trench's volume to be filled. The amount of oxide etched from the top corners of the wide and narrow trenches is not proportional to the volumes to be filled. Therefore, relatively more etched oxide helps to fill the narrow trench than helps to fill the wide trench. As a result, when an HDP-CVD process ends, the oxide layer filling and overlying the narrow trench is thicker than the oxide layer filling and overlying the wide trench. During subsequent CMP, more oxide is removed over the wide trench than is removed over the narrow trench due to CMP overpolishing ("dishing"). The following hydrofluoric acid anisotropic etch does not promote uniform SiO_2 thickness among the narrow and wide trenches. Accordingly, after HDP-CVD, CMP, and subsequent wet etch, the oxide thickness filling narrow and wide trenches is non-uniform. However, the SiO_2 often serves as a base for

subsequently deposited overlying layers. Since such overlying layers should be planar and have uniform thickness, it is desirable to deposit silicon dioxide such that the oxide thickness filling and overlying trenches of various aspect ratios on the same wafer is relatively uniform.

SUMMARY

HDP-CVD is used to deposit silicon dioxide over a semiconductor wafer in which trenches are formed. Oxygen and silane gasses react to form the deposited silicon dioxide. A high frequency bias signal is used to make plasma ions etch a portion of the deposited silicon dioxide at the top corners (cusps) of the trenches. The etching and the depositing of the silicon dioxide is controlled such that the etch to deposition ratio is 0.07 or less. In some embodiments this etch to deposition ratio is achieved by using an oxygen to silane ratio of 1.3 or less. Low etch to deposition ratio is also achieved by reducing the high frequency bias power used to etch the deposited silicon dioxide, and by reducing the total gas flow rate.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a cross-sectional view of an integrated circuit structure.

FIG. 2 is a graph plotting fill layer thickness variations versus etch to deposition ratio.

FIG. 3 is a graph plotting fill layer thickness versus trench width.

FIG. 4 is a graph plotting etch to deposition ratio versus silane to oxygen gas ratio.

DETAILED DESCRIPTION

Persons familiar with integrated circuit fabrication will understand that the drawings are not to scale, and that certain well-known features (e.g., specific layer fill shapes) have been omitted from the drawings so as to more clearly illustrate the invention. Embodiments were carried out using a SPEED tool manufactured by NOVELLUS, INC. of San Jose, California. Cross-sectional thickness measurements were measured on patterned semiconductor wafers by using a HITACHI model 5400 scanning electron microscope. Non-destructive thickness and thickness uniformity measurements were determined using an OPTIPROBE 2600 manufactured by THERMAWAVE of Fremont, California. Other tools may be used in accordance with the invention.

FIG. 1 is a cross-sectional view illustrating a typical thickness variation in an HDP-CVD deposited layer. Narrow trench 10 and wide trench 12 are formed in integrated circuit substrate 14 (e.g., wafer of monocrystalline silicon). Narrow trench 10 has an aspect ratio of at least 2.5 (e.g. 5000 Å deep / 1800 Å wide) and wide trench 12 has an aspect ratio of less than 1.0 (e.g., 5000 Å deep / 8800 Å wide). Layer 16 (e.g., polycrystalline silicon) and layer 18 (e.g., silicon nitride) are shown in FIG. 1 to illustrate that one or more layers may be formed over substrate 14, and that trenches 10,12 may extend through such layers. Active electronic devices such as transistors may be formed in substrate 14 or in layers overlying substrate 14. Metal layers patterned to form electrically conductive interconnects may also be formed over substrate 14.

Layer 20 (e.g., silicon dioxide) is formed over substrate 14 using an HDP-CVD process so as to fill the trenches 10,12. Layer 20 is illustrative of layers formed using an HDP-CVD process in accordance with the invention.

Such layers may be formed directly on the substrate, or overlying other layers such as polycrystalline silicon, silicon nitride, or metal formed over the substrate. In some embodiments layer 20 is doped using conventional P-type or N-type dopants. In other embodiments, layer 20 is not doped.

As shown in FIG. 1, the thickness of layer 20 overlying and filling trench 12 is defined between bottom surface 24 of layer 20. Similarly, the thickness of layer 20 overlying and filling trench 10 and top surface 28 of layer 20. FIG. 1 illustrates (in exaggerated scale) that the HDP-CVD process makes the thickness of layer 20 overlying and filling trench 10 larger than the thickness of layer 20 overlying and filling trench 12.

Since HDP-CVD both etches and deposits material, an etch to deposition (E/D) ratio is established for particular process parameters. The E/D ratio is the amount of material etched divided by the amount of material deposited. In one instance, the etch to deposition ratio is determined by using an HDP-CVD process to deposit SiO_2 on an unpatterned wafer for a particular time. The thickness of the deposited oxide layer is determined. Then, on another unpatterned wafer, the same HDP-CVD process parameters are used to deposit SiO_2, but the high frequency bias signal is turned off. The thickness of this second oxide layer is determined. The difference in the oxide layer thicknesses of the two wafers is the amount etched for a particular set of process parameters. The E/D ratio is determined by dividing the amount etched by the amount deposited under non-bias conditions. Etching due to HF bias was verified by using HF bias only on oxide wafers in the reaction chamber. After HF bias only conditions, the measured oxide thickness was less than the original thickness.

The inventors have discovered that thickness variations in an HDP-CVD deposited silicon dioxide layer filling both narrow (e.g., 1800-3300 Å) and wide (e.g., 6600-8800 Å) trenches of the same depth (e.g., 5000 Å) are controlled by minimizing the E/D ratio. The wide trenches are at least twice the width of the narrow trenches, so that the aspect ratio of the wide trenches is less than half the aspect ratio of the narrow trenches. Three process parameters in the HDP-CVD reaction chamber are used to control the E/D ratio: the ratio of oxygen to silane gas, the power of the high frequency bias signal, and the total gas flow rate (reacting and inert gasses) introduced into the chamber.

FIG. 2 is a graph showing a relationship (plotted as squares) between E/D ratio and oxide thickness variation in a layer filling an approximately 1800 Å wide trench and an approximately 8800 Å wide trench. Both trenches are about 5000 Å deep. As shown in FIG. 2, the inventors have discovered that the fill layer thickness variation between narrow and wide trenches begins to markedly decrease at an E/D ratio less than about 0.075. A thickness variation less than 390 Å is achieved using an E/D ratio of about 0.022.

FIG. 3 is a graph showing relationships between trench widths and fill layer thicknesses. The trench widths are plotted in the range of 0.0 - 1.0 micrometers (μm) along the horizontal axis and the fill layer thickness are plotted in angstroms along the vertical axis. Curve 300 (shown defined by the squares) is a plot showing thicknesses of an SiO_2 layer deposited in substrate trenches of various widths using an HDP-CVD process with an E/D ratio of about 0.07. Referring to FIGs. 1 and 3 together in one illustrative case, in which trench 10 is approximately 1800 Å wide and trench 12 is approximately 8800 Å wide, the oxide thickness difference is approximately 600 Å. In cases with other large trench

width variations, as illustrated by FIG. 3, the typical thickness difference between narrow and wide trenches is approximately 700-900 Å.

Curve 302 (shown defined by the plotted diamonds) is a plot showing SiO_2 thicknesses when deposited using an HDP-CVD process having a reduced E/D ratio of about 0.022. It can be seen that for various trench widths, the thickness differences are less than 400 Å--significantly less than for the 0.07 E/D ratio process used to define curve 300. In the case of 1800 Å and 8800 Å wide trenches, the thickness variation is about 200 Å.

The inventors have further discovered that a low O_2:SiH_4 ratio and a low power high frequency bias signal will achieve a desirable low E/D ratio in the HDP-CVD process. Reducing the total gas flow rate also helps to achieve the desirable low E/D ratio. FIG. 4 is a graph showing three relationships between an O_2:SiH_4 gas ratio plotted along the horizontal axis and an E/D ratio plotted along the vertical axis. The upper curve 400 (shown defined by the diamonds) is for an HDP-CVD process using a 2000 watt (W) power HF bias signal and 325 standard cubic centimeter per minute (SCCM) helium (He) gas flow rate. In this instance, He is used because He^+ ions are more effective than, e.g., Ar^+ ions to sputter etch the oxide deposited at the upper trench corners that helps to fill the trenches. However, other ions such as Ar^+ may be used in other instances. The middle curve 402 (shown defined by the squares) is for a 1500 W power HF bias signal and 325 SCCM He gas flow rate. The lower curve 404 (shown defined by the triangles) is for a 1500 W power HF bias signal and 200 SCCM He gas flow rate. For the conditions shown in FIG. 4, a chamber pressure of less than 6.3 millitorr is maintained during processing in the SPEED tool.

As shown in FIG. 4, for various HF bias signal power levels and various total gas flow rates, the E/D ratio begins to be reduced at an O_2:SiH_4 ratio of approximately 1.7, and is significantly reduced at an O_2:SiH_4 ratio of approximately 1.3. In some cases, illustrated by points 400a,402a,404a, this 1.3 gas ratio is achieved using an O_2 flow rate of approximately 170 SCCM and an SiH_4 flow rate of approximately 130 SCCM. The flow rates for other O_2:SiH_4 ratios are shown in TABLE I. It is also seen by comparing curves 400 and 402 that lowering the HF bias signal power lowers the E/D ratio when gas flow rates remain constant. By comparing curves 402 and 404 it is seen that lowering total gas flow rate reduces the E/D ratio when bias signal power and oxygen and silane rates remain constant.

TABLE I

O_2:SiH_4 Ratio	SiH_4 (SCCM)	O_2 (SCCM)
1.67	140	235
2.0	150	300
2.3	130	300

Referring again to FIG. 1, embodiments of the invention result in the difference between the layer 20 thickness over surface 22 and the layer 20 thickness over surface 26 is less than when using known HDP-CVD processes. Following deposition, in one embodiment layer 20 is polished using conventional CMP to expose the top surface of silicon nitride layer 18. Such CMP results in surface 32 over trench 10 and surface 34 over trench 12. Layer 20 is further etched using a conventional hydrofluoric acid etch to produce surface 36 over trench 10 and surface 38 over trench 12. In one case surfaces 46,38 are approximately 600 Å below top surface 40 of polycrystalline silicon layer 16.

Skilled artisans will appreciate that the specific embodiments disclosed herein are illustrative, and that many variations are possible. Embodiments are not confined to depositing silicon dioxide or silicon substrates. For example, embodiments may include an HDP-CVD process for phosphate silica glass (PSG), which may be used as the pre-metal layer dielectric. Embodiments may also be used for intermetal dielectric layer processes. Therefore, the scope of the invention is defined by the following claims.